FAST Digital IF Architecture and Open Standard Digital IF Interfaces

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***Abstract*—In expanding the vision of an all-digital SATCOM terminal, the CERDEC Space & Terrestrial Communications Directorate (S&TCD) sponsored a digital-IF working group focused on creating a core digital IF architecture for strategic SATCOM terminals and defining a series of modular open standard digital interfaces (OSDI). This paper describes that Future Advanced SATCOM Technology (FAST) architectural framework, consisting of a front-end Digital Conversion Subsystem (DCS) that performs real-time data conversion of 1 GHz of bandwidth, a Wideband Signal Processor (WSP) that performs real-time channelization / signal synthesis to a zero-IF signal, and finally a bank of Digital Modems (DM) that modulate/demodulate the baseband I/Q samples. It also outlines the framework for the FAST OSDI objects and classes defining both the VITA 49-based digital IF signal transport between subsystems and the supporting control infrastructure. Finally, the paper highlights trades for digital IF architecture extensions anticipated for strategic SATCOM terminals.**

Keywords—digital IF SATCOM; FAST OSDI

I. INTRODUCTION – FAST PROGRAM OVERVIEW

Future Advanced SATCOM Technologies (FAST) is a four- year research and development program sponsored by US Army Communications Electronics Research & Development Engineering Center (CERDEC) in FY12. The primary objective of the research and development conducted under FAST is to develop the next generation all digital architecture for strategic SATCOM, revolutionizing the realm of possibility. Historically, the evolution of the strategic SATCOM architecture has been relatively slow in comparison to the evolution of other telecommunications technologies (i.e. Personal Communications Devices (PCD) and Services). The component-level technology has significantly evolved over time, due to demands in other growing technological areas, however the system level technology has significantly lagged with regards to breakthrough innovation, predominately due to the strategic terminals lasting longer than the expected life cycle. FAST has taken the initiative to expedite innovation, by developing a suite of technology demonstrating the implementation of an all digital SATCOM terminal with the associated digital subsystems and corresponding applications. Through the early stages of the development process the need for standardization became a priority, as it became apparent that there are many variants an all digital SATCOM architecture can take on, depending on mission specific requirements. It also became apparent that the architecture's core subsystems can be functionally equivalent, but not interoperate when designed by different vendors. To potentially circumvent this problem, FAST initiated another effort to develop an Open Standard Digital-IF Interface (OSDI) for SATCOM Systems. This development focused on fostering open market competition while not limiting creative "black box" designs, non-proprietary technology, and designs that achieves compatibility-interoperability-interchangeability. This effort was a teaming effort involving CERDEC Space & Terrestrial Communications Directorate (STCD), Defense Information Systems Agency (DISA), Harris Corporation GCS, Comtech EF Data Corp., Welkin Sciences, Hughes Defense and Intelligence Systems, L-3 Communications West, and RT Logic. This effort has resulted in a modular architectural framework defining the signal processing elements and the subsystem communication interfaces to create a class of digital intermediate frequency (IF), or "all digital," strategic fixed SATCOM terminals. The resultant standard is currently undergoing verification and validation through prototyping. Upon successful verification and validation, the OSDI shall be published.

II. FAST ARCHITECTURE: SUBSYSTEMS AND OSDI

As a framework targeted towards fixed strategic SATCOM terminals, the open modular FAST architecture and OSDI are generally based upon multiband, single aperture, fixed strategic terminal architectures with mission requirements similar to those for the AN/GSC-39B, -49, -52, AN/FSC-78B/79B, and the Modernization of Enterprise Terminals (MET) fixed terminals [1,2]. The FAST architecture also incorporates compatibility with the modular open standard Government Reference Architecture [3], most notably the segmentation of data, signal, and control functions into distinct processing planes. The primary benefit of the FAST digital IF SATCOM terminal architecture is the ability to consolidate IF/baseband processing in low-cost digital hardware that, with the widespread adoption of software-defined platforms and programmable logic, can be dynamically loaded to meet evolving mission requirements. Secondary benefits may include new capabilities like reduction in the analog IF equipment suite, improvement in transmit noise spectral density, dynamic channel topology management, all-digital spectral monitoring, enhanced physical and logical separation of security enclaves, and advanced DSP capabilities, such as adaptive compensation, linearization, interference cancellation, and multi-aperture beam-forming

The contemporary functional architecture of an earth station includes much of the front end RF processing hardware already consolidated via block converters that provide an IF

interface to the modems (baseband signal processors). This IF boundary is the most logical analog-to-digital conversion interface when dealing with a large number of signals or large bandwidths, although some legacy modems will employ secondary IF conversions to 70/140 MHz. A generic functional diagram of a single digital communications link, tailored towards the signal plane processing within a strategic terminal, is shown in Figure 1.

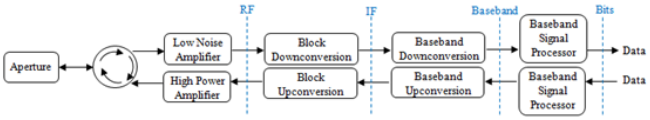

Figure 1. Signal plane processing in strategic Earth terminal

The processing shown is most notable for its mirror symmetry between the transmit and receive signals and, most critically, the absence of the analog-to-digital (ADC)/digital-to-analog (DAC) converters. While the ADC/DAC are among the most critical components in any digital communications link, their functional purpose is to act as a transducer that "optimally" changes the processing domain rather than change the actual content of the signal. For a single signal, the most efficient ADC/DAC location is generally at baseband (a zero-IF/ZIF modem) or at a nonzero low IF (e.g. 70 MHz, 140 MHz, 700 MHz) that enables sufficient oversampling of the analog signal to optimally process in the digital domain; the fundamental constraint on this sampling process is that of the Nyquist sampling criterion, dependent primarily on the instantaneous bandwidth of the actual communications signal. The scalability of this functional architecture to simultaneous processing of multiple signals, and the associated impacts of the ADC/DAC location within the architecture are the core drivers of the present model for digital IF SATCOM. The digital IF architecture must be capable of supporting point-to-point SCPC links, all varieties of communications links (SCPC, FDMA, TDMA, CDMA, MF-TDMA), distributed apertures, and also new desired capabilities for switching signal streams between distant terminals. A top-level view of the digital IF FAST architecture, capturing a single digital IF messaging stream (up to 1 GHz instantaneous bandwidth) as integrated into a notional fixed strategic terminal, is shown in Figure 2.

The architecture is composed of assemblies notionally located at an electronics building (EB), a pedestal, and the aperture/hub assembly. Functionally, the digital IF FAST architecture may be decomposed into an RF section (red) and the core digital IF processing components (gray). The terminal architecture for the RF section can be translated to the analog IF architecture definition in MIL-STD-188-164B [1], and the digital IF processing represents an aggregation of MIL-STD-188-165A [2] requirements for parallel modems. Supporting these core processing elements is an infrastructure for terminal controls (green), frequency and timing synchronization (purple), and user data interfaces (cyan). The rigid separation of the user signal plane (navy), the control plane (green), and the user data plane (cyan) adhere to the terminal segmentation as defined in the GRA 3.0 framework [3], helping ensure commonality with analog IF terminals.

The RF section includes block frequency translation to the L-band IF (1-2 GHz) in the block up-/down-converters (BUC/BDC), amplification in the high-power amplifiers (HPA), noise figure optimized wideband reception in the low noise amplifier (LNA), and potentially multiband feed assemblies integrated into a single aperture. The architecture diagram shown in Figure 2 offers insight to the potential for multiple RF bands, each interfacing to a unique digital IF

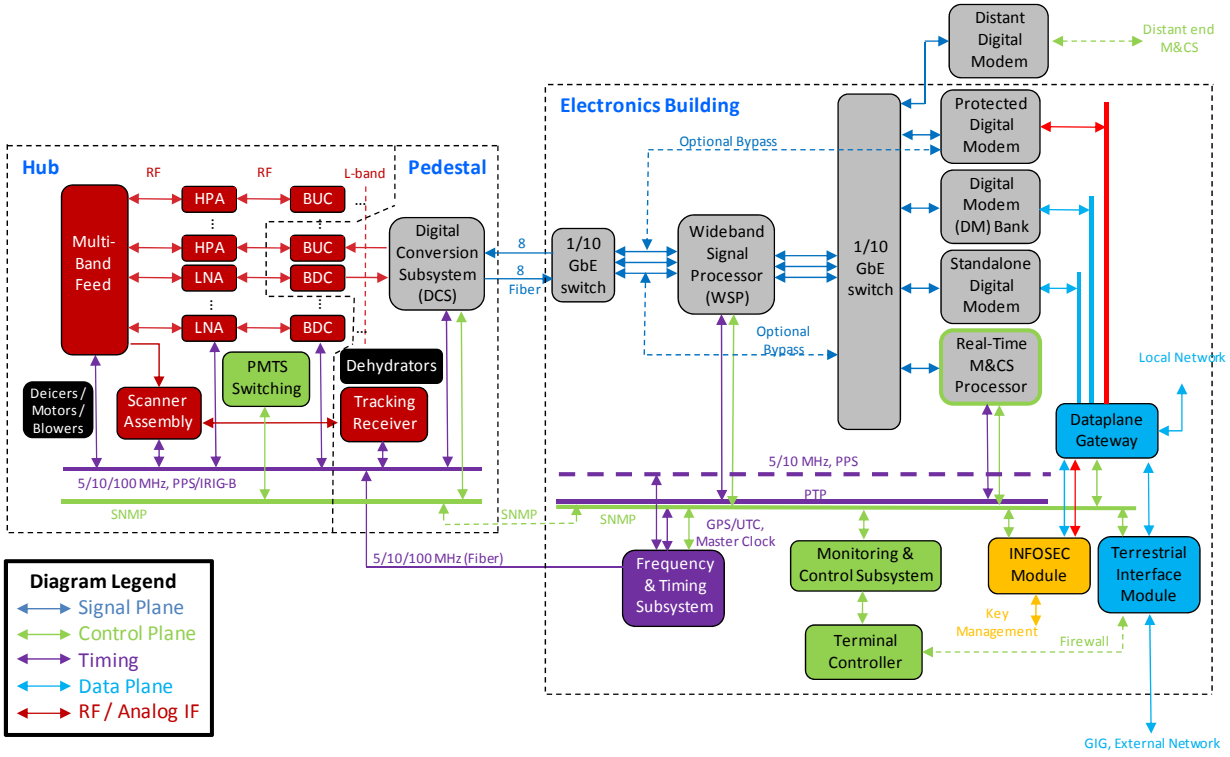

Figure 2. Top-level Digital IF SATCOM Architecture

digital conversion subsystem (DCS), although only one aperture is detailed out for simplicity. Additional RF functions within the hub/pedestal include the scanning/tracking receivers, mechanical/environmental regulation subsystems, and local test equipment (performance monitoring and test subsystem, PMTS) supporting real-time measurement of gain, flatness, and spectral characteristics. Given that the RF section is so similar to that of an analog IF terminal architecture, this paper focuses on the subsequent portions of the architecture; the most relevant characteristic is the IF input/output supporting up to 1 GHz of instantaneous bandwidth as supplied to the DCS.

The digital IF terminal processing section interfaces to the L-band IF signal, digitizes the wideband signal in the DCS, and transports the digitized wideband signals over Ethernet, using a VITA-49-compliant sample encapsulation to the wideband signal processor (WSP). The signal plane interface between the DCS and WSP conveys signals in digital quadrature format, limited in bandwidth only by the GbE transport mechanism. Routing of the different digital IF sample streams is supported with VLAN tagging to logically separate streams. The DCS, Ethernet switching, and WSP take the place of the fine-tune converters and L-band switching subsystem (LSS) in an analog IF architecture. Once signals are received, the WSP acts primarily as the system channelizer and gain control manager. The WSP also converts the filtered/rate-adjusted signals to quadrature baseband, reducing the signal sample rate to the banks of digital modems (DMs). "Rate adjustment" within the WSP involves increasing or reducing the sample rate of each sample stream in binary steps to a fixed set of sample rates; note that the actual signal bandwidth can be any value, with the sample rate chosen as the next "level" up to meet appropriate sampling criterion. The VITA-49-encapsulated sample streams [4] provided between the WSP and DM contain the carrier-specific baseband quadrature samples processed by the DM for signal transmission/reception. The DM is effectively a pure digital baseband processor, strictly producing/receiving samples at baseband. Within the digital IF transport sections of the FAST architecture, various opportunities exist for differential routing of quadrature sample streams among like components; i.e., the DCS can route portions or mirror images of the digitized spectrum to multiple WSPs (not shown) and/or the WSP could interface to multiple DCS entities in a distributed aperture architecture extension. Each of these core digital IF processing subsystems are described in subsequent sections along with the OSDI.

The supporting elements of the digital IF architecture are in many ways similar to the existing analog IF terminal types: the terminal control infrastructure is generally broken into three components: (1) the terminal controller (TC) acts as the terminal processor of frequency planning information, supporting centralized (e.g., "lights out") or local (intra-terminal control stations) control; (2) the monitoring & control subsystem (M&CS) centralizes subsystem-level configuration, automated calibration, intra-terminal diagnostics, control, performance monitoring, and alarm (CMA/PMTS) functions; and (3) the control plane network uses SNMPv3 [5] and precision timing protocol (PTP) [6] to communicate / synchronize the various subsystems under local control of the M&CS.

The FAST terminal infrastructure incorporates a frequency and timing synchronization subsystem (FTSS) that manages synchronization to the individual subsystems. The FTSS distribution to the RF front end equipment is similar to existing analog IF terminals with an analog reference (e.g., 1/5/10/100 MHz) that is generally phase locked for maintaining RF converter frequencies. As the primary digitizer in the terminal, the DCS receives the analog reference, supporting precision sample timestamping. The FTSS also distributes a 1PPS and 10 MHz references (as needed) for absolute timing to the hub/ pedestal subsystems, optionally encoded on the same RF cable as the primary frequency reference. Within the EB, migration to a digital IF enables coarser time synchronization employing the IEEE-1588 PTP [6], eliminating the traditional need for {5/10 MHz, 1PPS, IRIG} reference distribution. Given the current availability of PTP embedded Ethernet PHY and the requirement to continue support of legacy analog modems with legacy modem adapters (LMA), some FTSS requirements for analog reference distribution within the EB are retained and provisions will be allowed for analog synchronization of the WSP/DMs in early implementations of the FAST standard.

The INFOSEC Module shown in Figure 2 is a placeholder for future COMSEC/TRANSEC functions, notionally as a centralized INFOSEC controller supporting the banks of DMs. These core functions and interfaces are anticipated to be terminal-specific and are generally left to the implementer to select an appropriate risk management framework [3].

The user data plane elements are broken into two distinct elements, integrating and distributing the user data as received to/from the external global information grid (GIG) interface: (1) the dataplane Gateway serves the function of user data plane information routing, multilevel security (MLS) adjudication (if required), and any inherent data rate adaptation/buffering functions; and (2 the terrestrial interface module is envisioned as the terminal Gateway to the GIG and/or any other external data and control interfaces of the terminal. Due to the extensive number of user data interface types, only a limited definition of the user data plane is contained within the FAST architecture.

The final elements in the FAST architecture are a series of 'applications' that will support terminal automation, PMTS functionality, and other real-time processing. One example application shown in Figure 2 is the real-time M&CS processor employing hardware comparable to a DM (possibly a reprogrammable hardware fabric serving either function) and can selectively support real-time spectrum analysis, link power control algorithms, automated gain-flatness calibration, and/or related functions. The specific requirements and options for applications are still under development and anticipated to be included in a future revision of the FAST OSDI.

One of the core tenets of the FAST architecture is that the subsystems be interchangeable and adhere to the OSDI interface definitions, lowering the aggregate cost of the resulting terminals and also simplifying the requirements on vendors providing the subsystems. The functional decompositions of the subsystems and the top-level processing requirements are provided to define the logical boundaries of processing in the digital IF framework rather than impose any specific implementations.

At the core of the OSDI definition is a series of interface objects and classes. The objects represent core terminal functions and include the following:

- Connectivity (CON) Object: A control plane object enabling establishment, maintenance, and teardown of all of the linkages within the terminal. The CON object communicates to each of the subsystems via unicast SNMPv3 across the control plane and generally utilizes the M&CS as the link establishment master that maintains a record and health & status (H&S) indicators of all current linkages.
- Monitor, Control, and Alarm (MCA) Object: A control plane object that monitors performance, controls subsystem configurations, and handles alarm reporting for all failures. The MCA object communicates to each of the subsystems via unicast SNMPv3 across the control plane and generally utilizes the M&CS as the MCA manager. The MCA object within the M&CS may support an interface to the TC.
- Signal and Data Transport (SDT) Object: The signal plane object supporting higher layer protocols and VITA-49-compliant quadrature baseband signal transport within the digital IF processing elements (DCS, WSP, DM) of the FAST terminal. The FAST SDT definition both tailors the VITA-49 context class definitions to support strategic SATCOM signal reception and represents an expansion of the baseline VITA-49 standard to support transmit operations.
- Timing Reference and Synchronization (TIM) Object: A hybrid control plane/analog reference definition providing sustained synchronization for each of the subsystems. The TIM provides analog references to the front end RF equipment, DCS (digitizers), and legacy modems/adapters. The TIM also employs a strict master-slave adaptation of the IEEE-1588 PTP for communicating synchronization information to the digital subsystems (WSP, DMs).
- Test (TST) Object: A control plane object that supports the MCA via automated terminal metric collection, closed-loop link calibration, and in-series calibration of system-level terminal conditions (e.g. gain flatness requirements). The TST object incorporates many of the terminal functions for the RF front end PMTS and for the EB applications that support distributed testing.
- Dataplane Socket (DAT) Object: A user data plane interface object. Given the numerous user interface types and limited impact on the terminal signal processing, the DAT object definition is largely assumed to be terminal specific. The newer generation of DMs are assumed to employ a wired GbE connection, similar to the signal plane, although a wide range of legacy interfaces are known to exist and are supported.

Classes are specific instances of objects, inherent to a subsystem's contribution to the overall object. These classes are generally denoted using a "." notation, such that the class defining the signal plane portion to the connectivity object is CON.SDT. Descriptions of these objects, classes, and lower-level messaging protocols are included in subsequent sections.

III. SIGNAL DATA & TRANSPORT (SDT)

Signals represented in a Digital IF format are exchanged between subsystems in the FAST system via Ethernet interfaces. The FAST SDT Object definition is designed to support the transfer of digital I&Q signal samples between FAST subsystems. At the highest SDT protocol layer, signal samples are encapsulated in VITA-49 packets [4]. The SDT definition utilizes both baseline VITA-49 Digital IF packets as well as Digital IF Extension packets designed to support transport of I&Q signal samples in digital-IF streams. These sample carrying data packets within digital-IF streams are further encapsulated in RTP (to aid in the identification of lost packets) and transported as UDP datagrams over an IP network [7,8]. Because of the real-time nature of the data transfer, UDP is preferred over TCP in this application. The SDT protocol definition supports VLAN tagging to logically separate groups of digital-IF streams [9]. SDT packets are transmitted over a high-capacity Ethernet interface in a metered fashion, commensurate with the underlying source rate, in order to reduce the need for buffering in FAST subsystems and intermediate COTS switching devices. In addition to data carrying packets, the SDT interface also supports the transmission of meta-data in VITA-49 Context packets. Typically, no other major traffic component is allowed on the SDT interface (this excludes ARP, ICMP, and IGMP).

The SDT object includes connection and direction (i.e. TX or RX) specific protocol definitions for connections between DCS, WSP and DM subsystems. The SDT.DCS.WSP[1] and SDT.WSP.DCS wideband interfaces support transport of a composite digital-IF stream; whereas the SDT.WSP.DM and SDT.DM.WSP connections are designed to support transport of digital-IF carrier or multi-carrier streams. The definition of the SDT object does not target a specific terminal IF interface for the DCS analog connection. Likewise, the definition does not target a specific high-capacity GbE capacity for transport of the VITA-49 packets.[2] The VITA-49 signal payload is specified to support a fixed number of 16-bit (I and Q each) digital-IF samples. Specific sub-classes within in the SDT description have been included to support transport of digital-IF composite signals covering a 125 MHz band sampled at 150 Msps. When accounting for overhead, the required capacity is well matched to a 10 GbE link. Covering a 1 GHz band requires eight 10 Gbps lanes, which could be supplied with eight 10 GbE links, two 40 GbE links or a single 100 GbE connection. For simplicity, Figure 2 only shows a subset of the possible network capacities.

The traffic on the SDT interface of the narrow-band side of the WSP consists primarily of the digital-IF streams from one or more attached DM. Currently the narrowband SDT interface definition supports signal transport within one or more 125 MHz subbands. VITA-49 packet definitions are provided to allow exchange of samples between a WSP and a DM for a carrier residing within a subband. The narrow-band SDT interface was designed with the goal of having the SDT network capacity required by a DM be proportional to the bandwidth of the underlying sampled SATCOM carrier. This approach adds complexity to the WSP, but allows the number of DM supported to be constrained ultimately by satellite transponder bandwidth and not by capacity on the SDT local network, provided said network has enough capacity to support the available transponder bandwidth.

[1] "." order indicates DCS is the source and WSP the sink

[2] Payloads with common full-size MTUs of 1500 bytes were chosen.

For FDMA-only DM, the standard header information in a VITA-49 Digital-IF packet and Context packets suffices for directing the WSP on how to handle a digital-IF stream. However, for DM supporting MF-TDMA and other frequency-agile waveforms, stream-handling information is required to assure proper placement of the carrier signal in both time and frequency. The VITA-49 sample carrying packets on the SDT.DM.WSP interface include extended header information to support time-frequency placement. A similar problem occurs on receive, where again control information must be passed from the DM to the WSP to direct downlink stream-synthesis from the composite digital-IF stream received from the DCS. This control data includes an activation time to direct the WSP processing. The SDT interface description includes definitions of extended VITA-49 data packets to support transport of this receive control information.

The current SDT protocol is targeted towards the three major FAST OSDI subsystems (i.e. DCS, WSP and DM). We anticipate that these same interface SDT definitions may be adopted by other subsystems, such as digital-IF monitoring equipment. However, other subsystems in an extended FAST architecture are likely to require new SDT sub-classes with VITA-49 IF Packet headers and Context meta-data more suitable to the device-specific application.

IV. Monitor & Control Subsystem (M&CS)

The Monitoring and Control Subsystem (M&CS) is the primary internal controller for the digital IF terminal, managing device configuration, connectivity, atomic-level control & status (C&S), real-time signal analysis, and link power control across the control plane. The M&CS communicates across the control plane using SNMPv3 messages; these SNMP messages are lower in priority than any timing synchronization messages, yet the M&CS has the highest authority in sending commands to the individual subsystems. As the primary internal terminal control agent, the M&CS manages the authentication of devices and serves as a subsystem configuration oracle via the MCA class, establishes and maintains connections between subsystems via its CON class, and performs intra-terminal testing and calibration functions via its TST class. The top-level functions of the M&CS are captured in Figure 3. The three agents are command, control, and status is obtained via SNMP.

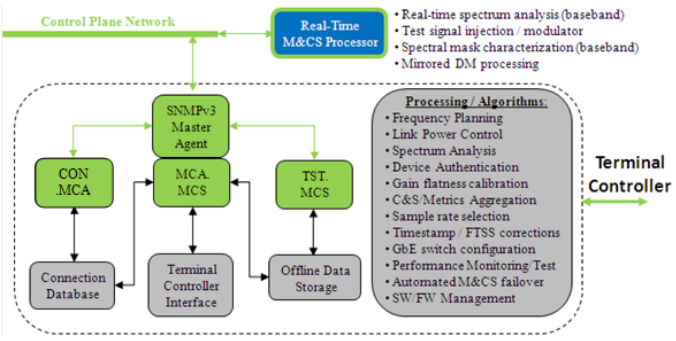

Figure 3. Monitor & Control Subsystem (M&CS) Components

The Connectivity (CON) Object is responsible for the configuration of all other system ports (such as those used for the high-speed SDT traffic) and is configured / maintained by the M&CS. The CON establishes and communicates port parameters between subsystems to support their affiliation. Port statistics from each of these connections are reported from the individual devices to the M&CS via the control plane (SNMP) and logged in an internal link status database.

The Test (TST) Object is responsible for specific terminal-level tests to be supported by the M&CS. Recommended tests are signal injection, spectrum analysis, gain flatness/deviation from linear phase calibration, and various loopback functional/performance tests. These tests are managed by the M&CS. Available tests include testing transmission paths between the Digital Modems (DM) and Wideband Signal Processor (WSP), and Wideband Signal Processor and Digital Conversion System (DCS). Upon initialization, devices in the system cannot host data payloads until they have successfully completed a self-test, validated themselves with the M&CS, and received a port configuration assignment from the M&CS.

V. Timing Reference and Synchronization (TIM)

While analog-to-digital conversions still require high-precision timing references, the introduction of all-digital modems with no analog front-ends reduces the necessity to widely distribute frequency references and UTC timing references. The FAST OSDI presents the trades for several terminal timing systems and recommends a transition from traditional analog to digital references in order to reduce costs related to distributing an analog network of timing signals, similar to the benefits of converting from analog IF to digital IF. Timing distribution methods discussed as part of the FAST OSDI consist of the following four architectures.

(1) Analog frequency references to all systems & analog UTC time (1PPS + IRIG) to all systems

(2) Analog frequency references for only the DCS and other RF terminal systems & analog UTC time (1PPS + IRIG) to all systems

(3) Analog frequency references for only the DCS and other RF terminal systems & digital UTC time (1PPS + NTP) to all systems

(4) Analog frequency references for only the DCS and other RF terminal systems & digital UTC time (IEEE 1588) to all systems

A reduced reliance on analog signals can be seen during each transition 1-4. Timing systems in traditional analog terminals most closely resemble the 1st architecture and it is reasonable to assume that this would be the expectation for what signals are available when digital IF systems first begin making appearances in terminals. The possibility also exists that early variants of modems will add a digital IF capability to an existing analog products. To minimize the impact of adding the Digital IF capability it is unlikely that the analog frequency references would be eliminated at this point. However, modems that are developed exclusively to pass digital IF signals would no longer require the analog frequency references and total number of analog frequency references that would need to be supplied could be reduced, creating a natural evolution into the 2nd architecture.

Newly developed terminals and retrofits are envisioned to mostly eliminate the reliance on analog modems. However, they can maintain ability to support a subset of analog modems through the use of legacy modem adapters to convert their signals to be translated to digital IF. As a result, a subset of analog frequency references must still be made available for the legacy modems and to perform analog to digital conversion by legacy modem adapters.

Architectures 3 and 4 introduce evolutions for the UTC timing signals to transition to digital, Ethernet based solutions. NTP in particular is a predominant timing standard used to synchronize the clocks of desktop computers across the internet. However, since the accuracy of NTP is at best 1 ms, 1 PPS would also be necessary to improve timing precision to meet the synchronization needs of the system with an accuracy of 1 µs or less. IEEE 1588, also known as PTP is an improvement over NTP. While PTP is also carried across Ethernet networks, the protocol stack operates at a lower level of the Ethernet stack than NTP and directly interfaces with hardware timers to maintain timing precision in the sub-microsecond range. Notionally, the PTP timing signals could be transmitted across the M&CS plane, through PTP-aware switches, eliminating the need for a separate network for timing signals all together.

VI. Test (TST) Object

Traditional signal monitoring techniques for analog terminals involve the use of RF cable patching and signal splitting to either view signal characteristics by spectrum analyzer or power meter, or to inject test signals with generators. The test object identifies new methods for monitoring and injecting signals for mostly digital systems and interconnections. Additionally, loopback capabilities are incorporated to allow for fault isolation to specific elements or signal paths.

Figure 4 highlights five test segments as part of the FAST terminal architecture with the signal flow of the TX and RX paths from the DM to the DCS indicated by the yellow arrows. Notionally, the M&CS coordinates the activation and de-activation of test functions in order to minimize the disruption to active links as part of the system. This digital architecture also introduces the capability of scheduling routine system integrity checks of inactive circuits or hot-standby units. Unlike traditional analog designs, digital IF signals being transported across Ethernet can be isolated on unique VLANs or multicast to multiple sources for monitoring purposes.

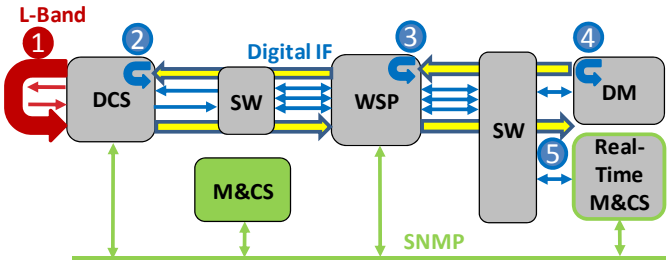

Figure 4. Loopback testing in a Digital IF terminal

L-Band loopback capabilities (1) exist at the DCS, similar to what is traditionally available for legacy modems with analog IF interfaces. Test tool such as power meters and spectrum analyzers natively support this analog interface for characterizing system signal outputs. The potential also exists to loopback transmit outputs to a hot-standby DCS in order to resample outgoing signals locally without disturbing active receive links. Similar loopback verifications can be performed using a non-active transmit path in order to verify the integrity of all elements and interconnections forming a link prior to transmission over the air. Digital IF loopback capabilities (2 and 3) assist with verifying the integrity of interconnections and the proper configuration of devices in the system without the need to perform any manual re-cabling which would be needed at the L-Band interface (1). Digital modems with compatible TX and RX modulation schemes would also notionally possess the capability to loopback digital IF signals at the Ethernet MAC layer as part of their built-in self-test (BIST).

While it is common to monitor the entire transmitted or received signal from an antenna, it is occasionally necessary to view the signal characteristics of an individual modem as well as injecting CW or multi-carrier signals during performance testing and verification. The real-time M&CS (5) connection to the Ethernet switch provides this monitoring and signal injection capability. The Ethernet switch can be configured by the M&CS to mirror ports to multiple devices, or digital IF streams can be configured to use multicast UDP streams in lieu of unicast. The real-time M&CS notionally would consist of a high-speed interface capable of capturing packets at line-rate, and performing an FFT or similar function based on the desired monitoring capability. Injection of multiple carriers upstream may be done by instantiating multiple digital IF streams with contextual information indicating the desired signal frequencies and power levels.

VII. Architectural Options and Extensions

The current FAST OSDI includes provisions for handling dropped digital-IF packets on either the wideband or narrowband SDT interface; forward error correction (FEC) is optional. Provisions have been made in the FAST OSDI to support (FEC) on the SDT interface. While the FAST OSDI does include a discussion of many of the issues related to implementing FEC on the SDT network, a specification of a particular FEC approach was not included in the initial release of the FAST OSDI. Specification of FEC was delayed until the FAST OSDI Working Group develops a better understanding, primarily via lab experiments using FAST subsystem prototypes, of how COTS switching equipment will respond to anticipated SDT network traffic loads.

The baseline FAST OSDI may be readily extended to support applications beyond conventional satellite ground terminals. We anticipate future extensions will include support for DM combining of digital-IF streams from multiple apertures. Digital-IF transport is ideal for aggregating signal from widely spaced apertures at a common processing node. In addition to aperture combining, long-haul Digital-IF transport has the potential to allow traffic load balancing between ground terminals. The FAST OSDI outlines additional extensions, including support for digital-IF monitoring equipment, digital-IF channel simulators, digital-IF test signal generators and legacy modem data converters, which would allow carrier signals from existing analog modems to be routed over a digital-IF network

VIII. Conclusions

All Digital SATCOM is the logical “next-step” for strategic SATCOM. Using the “Smart Phone Evolution” Paradigm, PCD/S has evolved at a rapid pace. In the span of ten years the technology has gone from multiple low-bit rate low-level of

sophistication devices, to a single high bit rate highly capable smart phone or tablet. Although the consumer market drives this pace, the underlying technology that allows the technology to flourish, is built on top of standards for EDGE, LTE, 4G etc. These standards enable the continuing innovation to further enhance the capabilities the devices can deliver. Strategic SATCOM is long overdue for a technological "face lift", and evolve much the way the smart phone technology has. It is envisioned that the body of work that has gone into developing OSDI, will help proliferate the development of Digital IF SATCOM systems and terminals. OSDI will serve as the starting point to help instantiate the implementation of all digital SATCOM architecture, from which further standards can either be derived or extended.

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